Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-14 (Cancelled).

Claim 15 (Currently Amended). A delay lock loop apparatus for use with an externally generated clock signal comprising:

a delay device comprising a first delay element and a second delay element, wherein the first delay element is configured to generate a first output responsive to a control signal and a first input, and wherein the second delay element is configured to generate the first input responsive to the externally generated clock signal and a set signal related to the frequency of the externally generated clock signal, wherein the second delay element comprises ~~a low frequency delay element for lower frequencies of the externally generated clock signal and a high frequency delay element for higher frequencies of the externally generated clock signal, wherein the low frequency delay element and the high frequency delay element are configured for operation at different frequency ranges of the externally generated clock signal~~ different second delay elements in discrete steps for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal,

wherein the delay device further comprises a frequency detection unit having an output signal used to adjust the at least one second delay element such that a second delay time is set in the second delay element as a function of the frequency of the first input, and

wherein the second delay element for low frequencies and the further second delay element for high frequencies are switched over for different frequency ranges of the externally generated clock signal,

a feedback device operably connected to the first delay element and configured to generate a time delayed first output, the feedback device operable to delay the first output by an amount substantially equal to a receiver time delay plus a driver time delay,

a phase difference detection device configured to generate signal responsive to the phase difference between the time delayed first output and the externally generated clock signal, and

a frequency detection unit configured to generate the set signal responsive to the frequency of the externally generated clock signal.

Claim 16 (previously presented). The apparatus of claim 15, wherein the first delay element is responsive to a filtered control signal, and wherein the apparatus further comprises,

a filtering device operably connected to the phase difference detection device and the first delay element.

Claim 17. (Cancelled).

Claim 18. (Cancelled).

Claim 19. (Previously Presented). The apparatus of claim 15, wherein the delay device comprises a controllably variable capacitor element.

Claim 20. (Previously Presented). The apparatus claim 15, wherein the delay device comprises a controllably variable current inverter.

Claim 21 (Previously Presented). The apparatus of claim 15, wherein the delay device comprises an inverter chain.

Claim 22 (Currently Amended). A method of providing clock signals to a circuit, the method comprising the steps of:

providing a delay control apparatus comprising a first variable delay element and at least one frequency variable delay element,

detecting the frequency of an external clock signal,

adjusting the time delay of the at least one frequency variable delay element based upon the frequency of the external clock signal,

delaying the external clock signal with the at least one frequency variable delay element and providing the delayed external clock signal to the first variable delay element, wherein the frequency variable delay element comprises ~~a low frequency delay element for lower frequencies of the externally generated clock signal and a high frequency delay element for higher frequencies of the externally generated clock signal, wherein the low frequency delay element and the high frequency delay element~~ different second delay elements in

discrete steps for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal,

wherein the at least one second delay element is adjusted by means of an output signal of a frequency detection unit such that a second delay time is set in the second delay element as a function of the frequency of the first input, and

wherein the second delay element for low frequencies and the further second delay element for high frequencies are switched over for different frequency ranges of the externally generated clock signal,

further delaying the delayed external clock signal with the first variable delay element by an amount of time equal to a receiver time delay plus a driver time delay,

providing the further delayed external clock signal to a feedback device,

time delaying the further delayed external clock signal with the feedback device, detecting the phase difference between the time delayed external clock signal and the external clock signal,

generating a control signal based upon the detected phase difference, and

controlling the time delay of the first variable delay element with the control signal so as to reduce the detected phase difference.

Claim 23 (Cancelled).

Claim 24 (Cancelled).

Claim 25 (Previously Presented). The method of claim 22, further comprising, before the step of detecting the frequency of an external clock signal, the step of:

resetting the delay control apparatus with a reset pulse.

Claim 26 (Previously Presented). The method of claim 22, wherein the step of providing at least one frequency variable delay element comprises

providing a first frequency variable delay element responsive to control signals related to a first frequency and a second frequency and not responsive to control signals related to a third frequency, and

providing a second frequency variable delay element responsive to control signals related to the second frequency and the third frequency and not responsive to control signals related to the first frequency.

Claim 27 (Cancelled).

Claim 28 (Previously Presented). The method of claim 22, further comprising the steps of:

providing a filtering device, and

filtering the generated control signal.

Claim 29-33 (Cancelled).

Claim 34 (Previously Presented). The apparatus of claim 15, wherein the frequency detection unit is operable to generate the set signal independent of the first output signal.

Claim 35 (Previously Presented). The apparatus of claim 34, wherein the first delay element is responsive to a filtered control signal, and wherein the apparatus further comprises a filtering device operably connected to the phase difference detection device and the first delay element.

Claim 36 (Previously Presented). The apparatus of claim 34, wherein the delay device comprises a controllably variable current inverter.

Claim 37 (Previously Presented). The apparatus of claim 34, wherein the delay device comprises a controllably variable current inverter.

Claim 38 (Previously Presented). The apparatus of claim 34, wherein the delay device comprises an inverter chain.